Doherty techniques for 5G RF and mm-wave Power Amplifiers

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1. Introduction

5G poses severe challenges to PA design. In the first place, output power and efficiency are of prime importance because of battery lifetime. The tradeoff between linear output power and efficiency is typically challenged by the high PAPR due to QAM modulation and/or OFDM techniques. But this important trade-off is challenged even more in 5G due to the high bandwidth requirements. Furthermore, the shift to higher frequencies, where more unused spectrum is available, also puts a burden on the overall PA architecture.

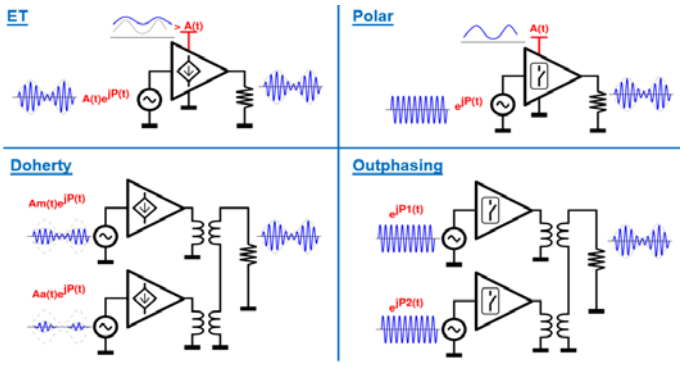

Figure-1: overview of different CMOS RF PA techniques: Envelope tracking (ET), Polar Modulation, Doherty and Outphasing

Figure 1 shows an overview of different CMOS PA techniques. Note that some PAs are switching (Polar and Outphasing) and some PAs work as linear PAs (ET and Doherty). Also note the properties (AM, PM) of the different signals that are being applied to the different PAs.

The major drawback of Polar and Outphasing, is the bandwidth expansion that occurs when converting I/Q signals into a polar format or an outphased format. Polar has an additional drawback that the envelope signal is a high power signal that requires a switching converter to maintain high efficiency. Outphasing is excellent to improve linearity at high output powers, but typically suffers from reduced linearity at low output power where two large signals are subtracted to achieve low output power. As such, Doherty seems to be a promising architectures and a good compromise between output power, linearity, efficiency and gain.

2. Doherty PA

A Doherty PA, proposed by William Doherty in 1936, combines two linear PAs through a combiner. When low output power is needed, the *main* PA is active, typically working as a linear Class AB type of PA. When a signal peak occurs and the main PA runs into compression, a second PA, the *auxiliary* PA, is turned-on to accommodate the need for more output power. If we ensure that the auxiliary PA does not consume DC power when turned off, the overall efficiency of this system can be increased compared to a regular Class AB PA which has the same output power. One way to achieve this, is an auxiliary PA that is biased as a Class C PA.

But there is more; in the Doherty PA the two amplifiers, main and auxiliary, are combined through an impedance inverter. This inverter, typically implemented with a quarter wavelength transmission line, ensures that the load impedance of the main PA reduces when the peak PA turns on. As such, when the main PA goes into compression and the auxiliary PA turns on, the output power of the main PA can still further increase since the auxiliary signal will work as a load-pull on the main PA, reducing its load and ensuring a further increase in (linear) output power.

But in CMOS, it is not easy to implement a quarter wavelength TLine. The loss would simply be too high, diminishing the benefit of a Doherty PA architecture. Therefore, in [1], the series combining transformer was proposed as a way to implement a Doherty PA. Although the load-pull effect is somewhat reduced compared to a traditional Doherty, the benefit of combining a Class AB with a Class C still results in a higher overall efficiency.

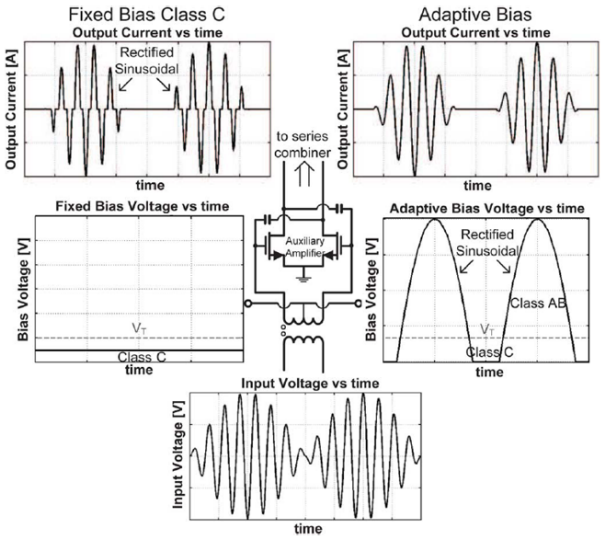

Figure-2: Active Class C to improve the Doherty performance in CMOS

A major challenge is to implement a Class C in CMOS. Indeed, biasing the transistor below the gate threshold voltage VT (as needed for Class C) would make the gm very small, which in turn requires a very large transistor size W and therefore high amount of parasitic capacitance. Although this capacitance can be tuned-out, it will always results in lower efficiency and lower bandwidth. And bandwidth is important for 5G.

Therefore, instead of using a normal Class C, it is far better to implement an active Class C, where the gate bias voltage (VGS) is kept low in the low power region, but is turned high when the auxiliary PA needs to deliver power to the output (see figure 2). The required VGS can be set with an analog power detector or can be calculated in the digital part of the transceiver. The bias voltage is basically proportional to the envelope signal and will therefore, just like in ET or Polar, have a much larger bandwidth than the I(t) or Q(t) signals itself. And as we go to higher bandwidths in 5G, the bandwidth of this active bias signal will only become larger. But one must remember that this bias signal is not a power signal and only needs to charge and discharge the gate voltage of the Class C PA. As such, it is much easier to generate this wideband envelope bias signal for a Doherty PA, compared to ET or Polar.

3. Doherty Implementations in 40nm CMOS

In [2], a Doherty PA was implemented in 40nm CMOS for LTE applications. The basic idea of this PA is shown in figure 3.

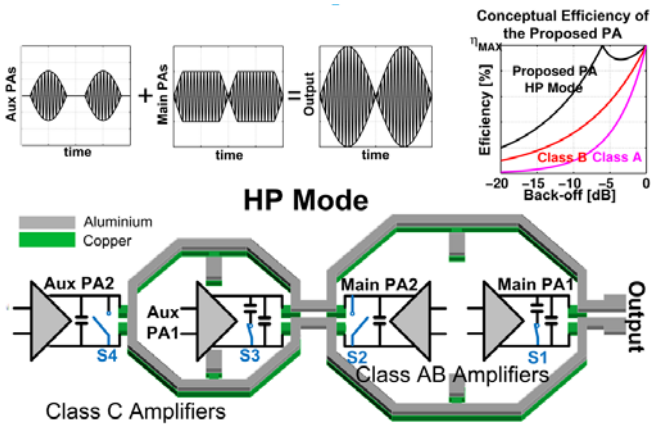

Figure-3: Doherty PA in 40nm CMOS

Key element in this design is the output transformer, which enables the PA to operate both in a high output power mode, and a low output power mode, and also implements the combiner functionality needed for Doherty operation. Although the load-pull effect is not that pronounced in this PA, the Class AB + Class C functionality is clearly present as shown in figure 3. This PA meets the LTE specifications and at back-off is comparable with more costly implementations as shown in Table 1.

Table 1: performance comparison

	Gain [dB]	P_{MAX}# [dBm]	PAE@ P_{MAX} [%]	PAE@ P_{MAX}-6 dB [%]	PAE@ P_{MAX}-12 dB [%]	Fully Integrated?	Technology, Supply [V]	Technique
C.Yunsung [MTT13]	24 /11*	27	37	22	21*	No	180nm CMOS + InGaP/GaAs,3.4V	dual mode envelope tracking (dual chip)
R. Wu [JSSC13]	17	27.9	40.2	20	10	No	0.35µm BCD + 0.35µm SiGe, 5V	envelope tracking (dual chip)
L. Yan Li [MTT11]	17	24.3	42	18	6	No	0.35µm SiGe BiCMOS,4.2V	envelope tracking
K.Onizuka [ISSCC13]	12	21.3	18	13*	5*	Yes	65nm CMOS, 3.3V	envelope tracking
This work	**21.3 /18.2***	**23.4**	**23.3**	**18.4***	**11.1***	**Yes**	**40 nm CMOS,1.5V**	**Doherty + Mode Switching**

P_{MAX} is defined as the measured average output power for which the ACLR1, ACLR2 and EVM specs are met.

Another Doherty PA implementation in 40nm CMOS, targeting mm-wave communication at E-band, is presented in [3]. Again, the performance at back-off exceeds the state-of-the-art. One of the key points of using mm-wave frequencies for 5G is the higher available bandwidth, and therefore, the Doherty has again a benefit compared to ET, Polar or Outphasing.

Conclusions

CMOS PAs remain a topic of intense research interest. Moreover, SOI technology allows the integration of the PA with the front-end module, further increasing the importance of making the right choice in topology for CMOS PAs. Also MIMO is key in this regard since it typically results in a lower power for each individual PA, making CMOS PA again feasible also for 5G.

A Doherty PA is the perfect candidate for medium power 5G fully integrated CMOS PAs, either in bulk or SOI. It can support high modulation bandwidth and good linearity and allows full integration as required for low-cost.

Acknowledgements

This work was supported by the European Commission in the framework of the H2020-ICT-2014-2 project Flex5Gware (Grant agreement no. 671563)

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